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February 23, 2009

The Circuit Design Company
 600 W Roush St
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Dear Mr. Setag:

You are in luck; this complicated circuit can indeed be simplified. My partner, Juan, and I have been able to design a circuit that produces the same output and should be much more cost effective than the one you provided me with. Since you asked for the details of how we accomplished this, we will provide you with those first and then show you the circuit we designed. The overall process was to find the logical expression for the circuit, then construct its truth table, then develop an expression with the same truth table, hopefully simpler, and then draw the circuit with that expression. These steps are discussed in more detail below.

The first step we took in simplifying the circuit was to figure out the logical expression that the circuit represents. By logical expression we mean writing the circuit out in terms of variables for each input, in this case P, Q, and R, and conjunctive and disjunctive operators, and, or, and not. The symbol for and is \wedge , the symbol for or is \vee , and the symbol for not is \sim . Using this information, we rewrote the circuit you provided as the following expression:

$$[(\sim P \wedge Q) \wedge R] \wedge [(P \vee \sim R) \vee (\sim Q \vee \sim R)].$$

The next step we took was to construct the truth table for this expression. It was our hope that by seeing the output of the truth table we would be able to get a better understanding for how the circuit was behaving and perhaps come up with an idea for how to make it simpler. The truth table for this expression is shown below.

P	Q	R	$\sim P$	$\sim Q$	$\sim R$	$(\sim P \wedge Q)$	$(\sim P \wedge Q) \wedge R$	$(P \vee \sim R)$	$(\sim Q \vee \sim R)$	$((P \vee \sim R) \vee (\sim Q \vee \sim R))$	$((\sim P \wedge Q) \wedge R) \vee ((P \vee \sim R) \vee (\sim Q \vee \sim R))$
T	T	T	F	F	F	F	F	T	F	T	F
T	T	F	F	F	T	F	F	T	T	T	F
T	F	T	F	T	F	F	F	T	T	T	F
T	F	F	F	T	T	F	F	T	T	T	F
F	T	T	T	F	F	T	T	F	F	F	F
F	T	F	T	F	T	T	F	T	T	T	F
F	F	T	T	T	F	F	F	F	T	T	F
F	F	F	T	T	T	F	F	T	T	T	F

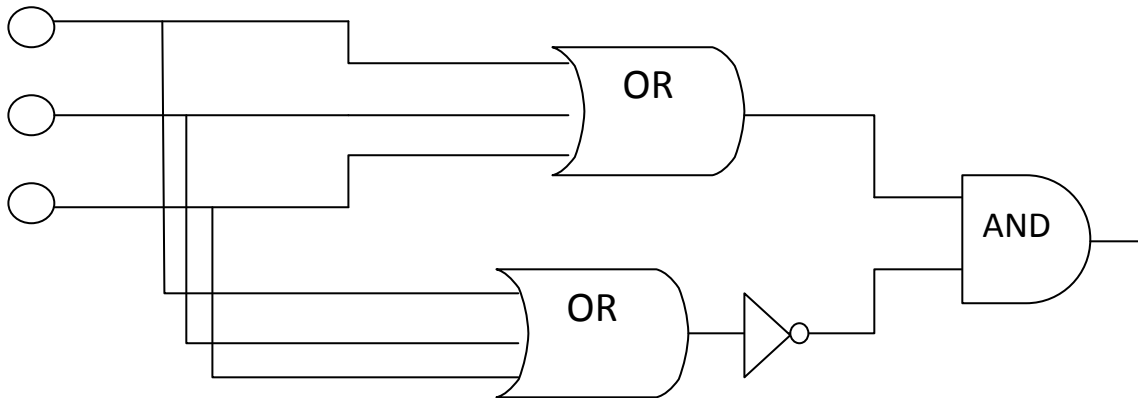
We represented a one with truth value T and zero with truth value F. As can be seen, no matter the value of the input, the output of the circuit is always false. (I don't mean to question your design team, but what kind of circuit is always off?) The fact that the truth table resulted in a contradiction (meaning false in all cases) made simplifying the circuit that much simpler. One way to obtain a contradiction is to AND together an expression and its negation. This is exactly what we did. Because your circuit requires three inputs, we combined them all with or and then combined that with an and of the negation of itself. If that is unclear, the logical expression is shown below.

$$[\sim (P \vee Q \vee R) \wedge (P \vee Q \vee R)]$$

To prove that these two expressions are logically equivalent, we constructed the truth table for this expression also. Two expressions are logically equivalent when the output of both truth tables is identical. So to show you that they are identical, the truth table for this expression is shown below.

P	Q	R	(PvQ)	(PvQ)vR	~((PvQ)vR)	(~(PvQ)vR) ^ ((PvQ)vR)
T	T	T	T	T	F	F
T	T	F	T	T	F	F
T	F	T	T	T	F	F
T	F	F	T	T	F	F
F	T	T	T	T	F	F
F	T	F	T	T	F	F
F	F	T	F	T	F	F
F	F	F	F	F	T	F

As you can see, both truth tables result in all false outputs, or a contradiction. Thus the two expressions are logically equivalent. So now when we draw the circuit for this expression, we know it will produce the same output as the one you provided us with. The circuit we developed is shown below.



As you can see, this circuit is much simpler. We were able to get rid of five unnecessary gates and still develop a circuit with the same output. I hope this new design will better fit your specifications and the description for how we came up with it will help you in future cases. If you have any more questions about simplifying or designing digital logic circuits, the book *Discrete Mathematics with Applications* by Susanna S. Epp is very helpful.

Yours Sincerely,

Group Y
Discrete Mathematicians